

PRIOR ART

FIG. 1

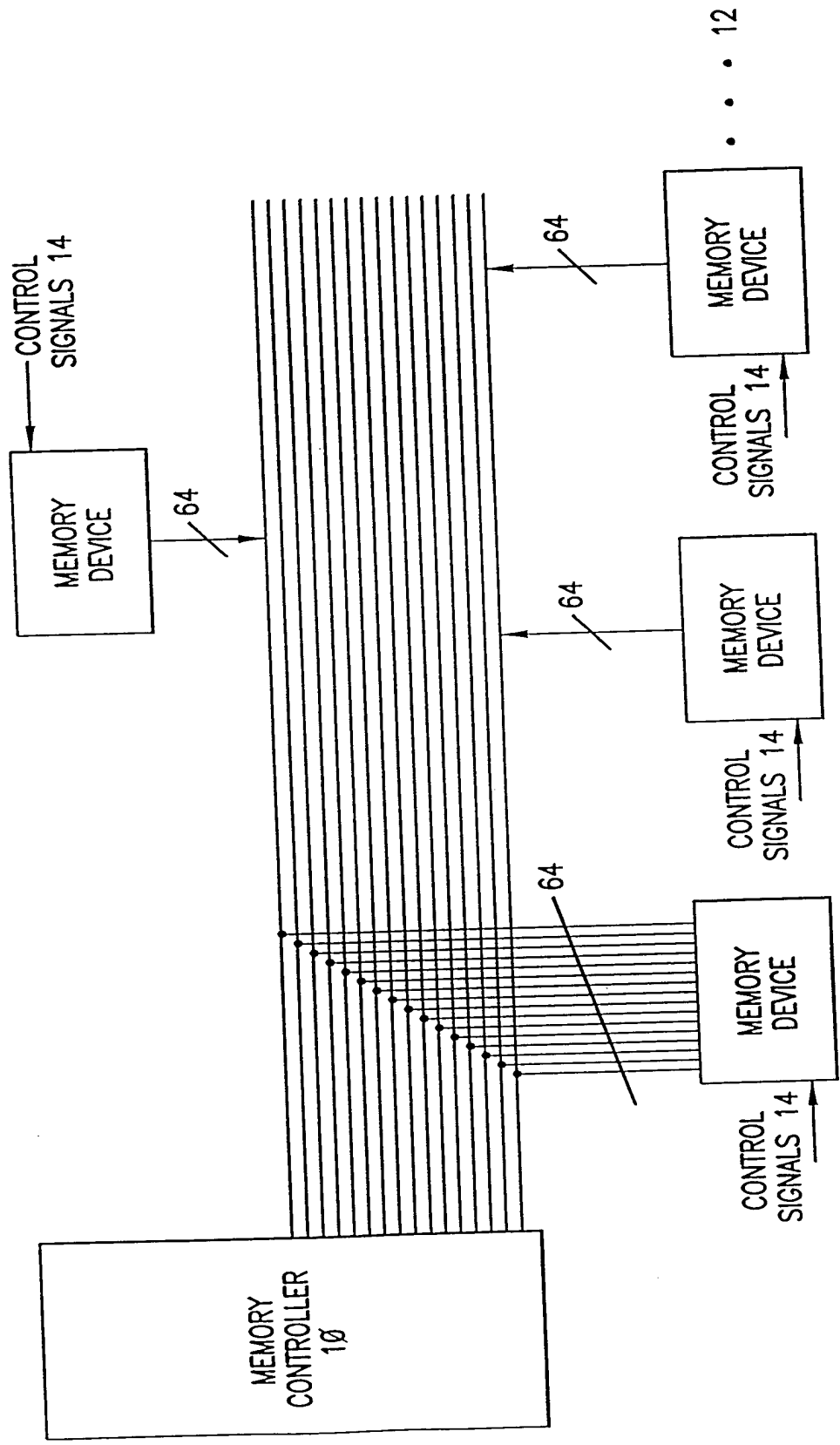


FIG. 2

PRIOR ART

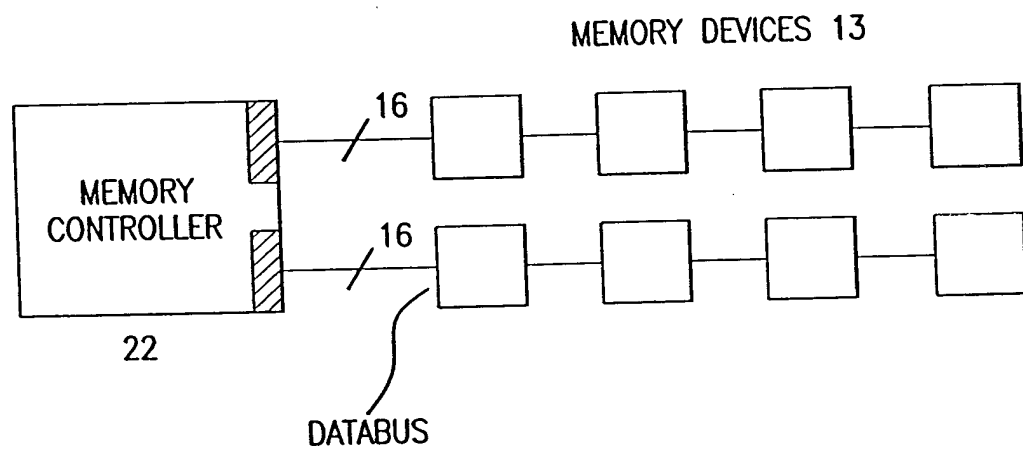


FIG.3

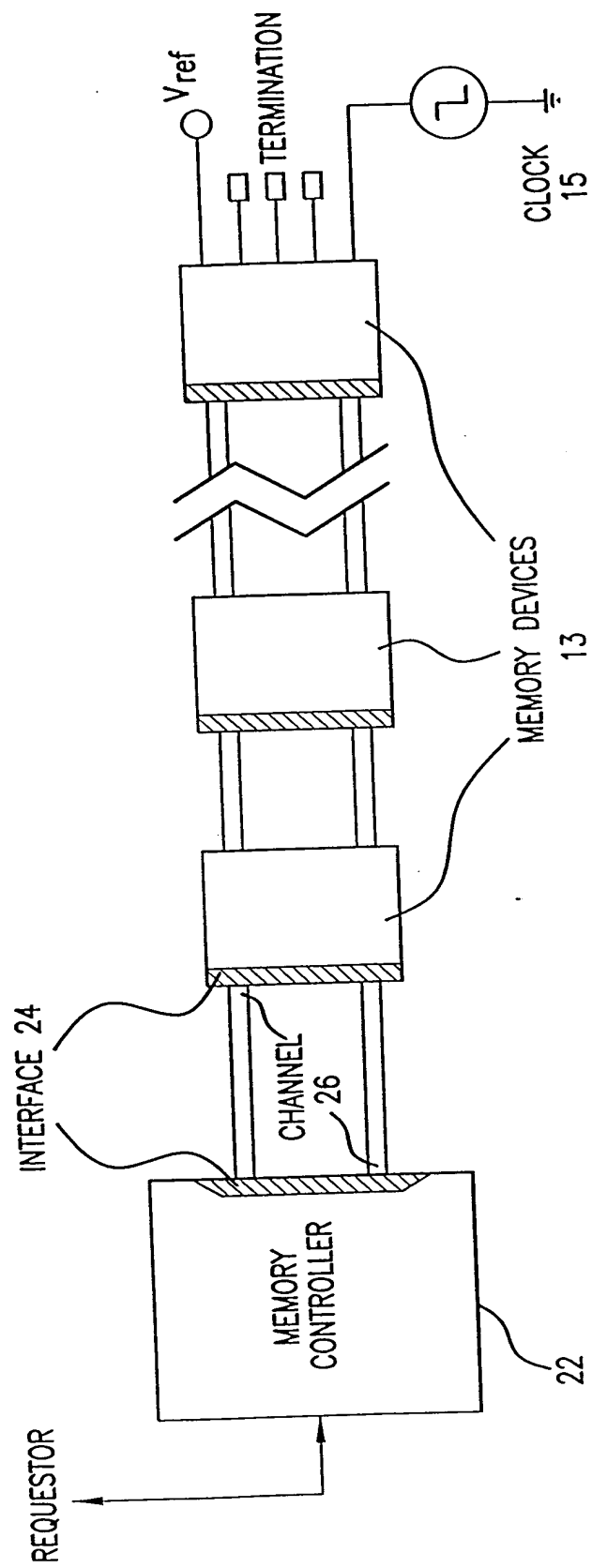


FIG.4

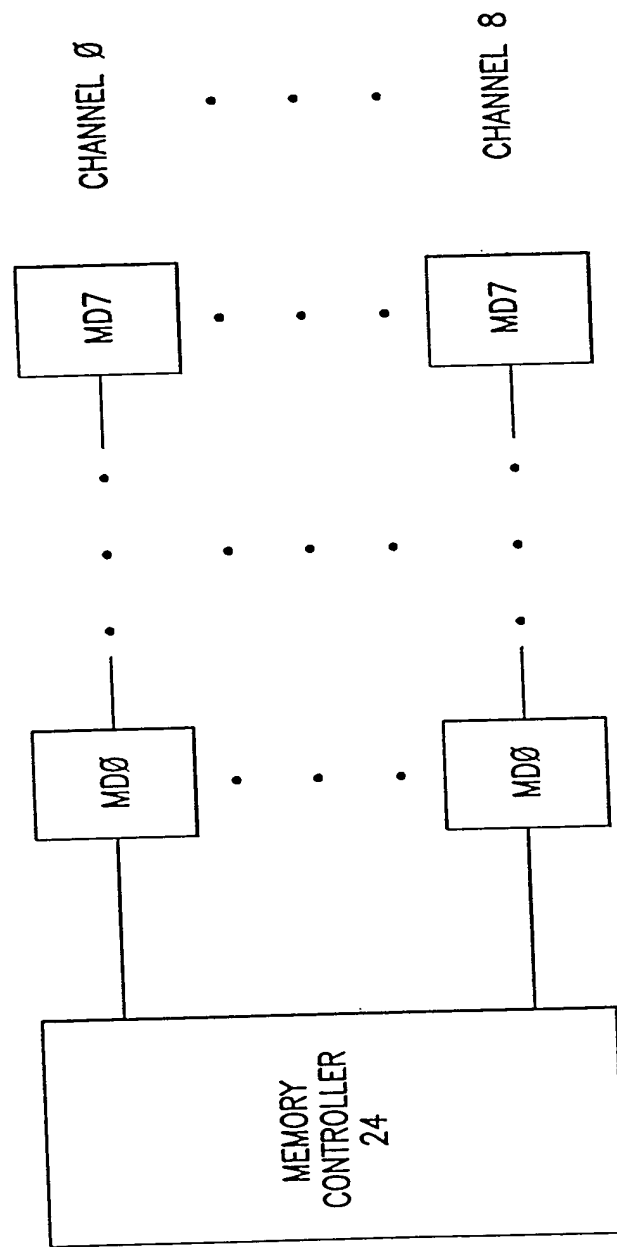


FIG. 5

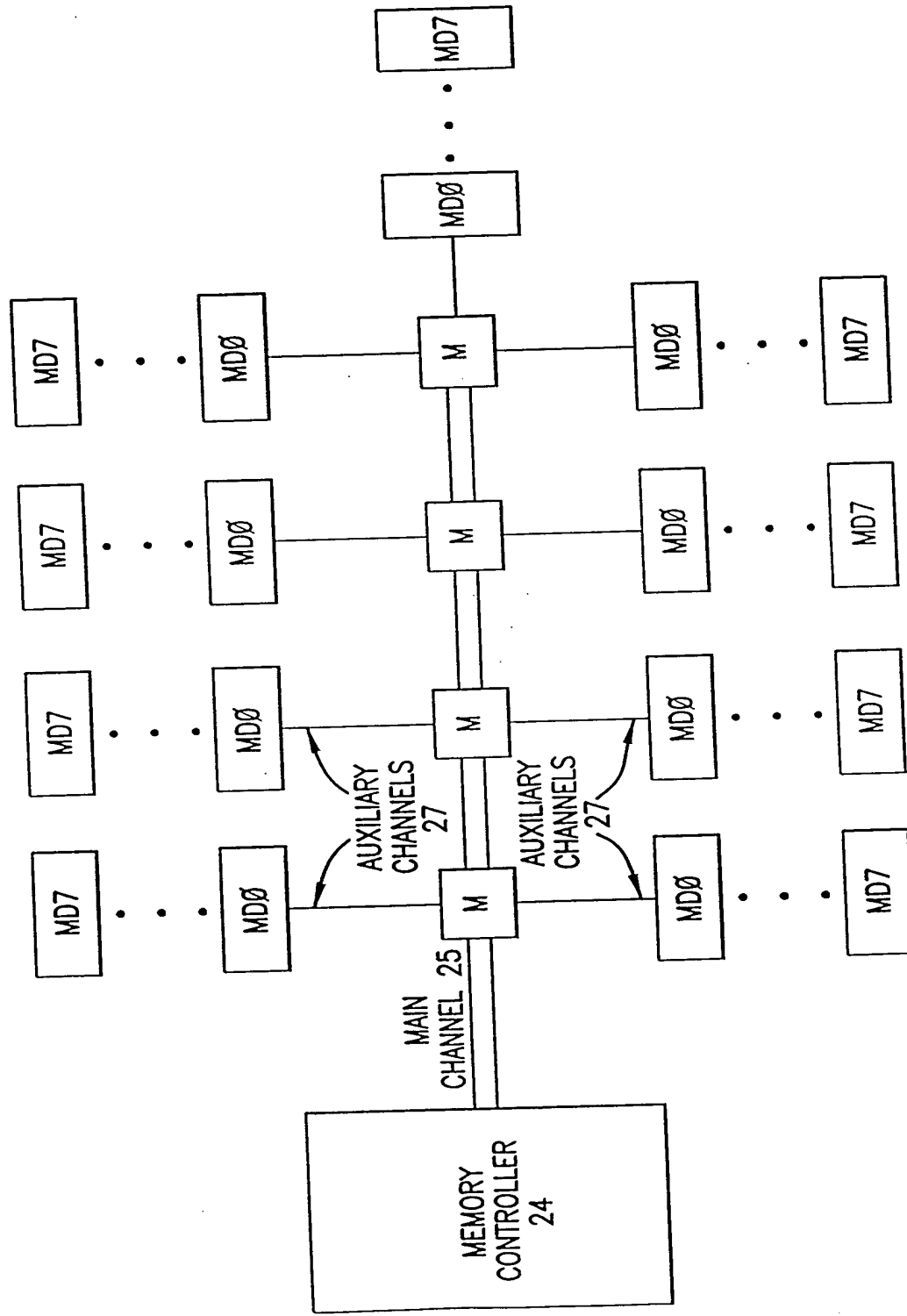


FIG. 6

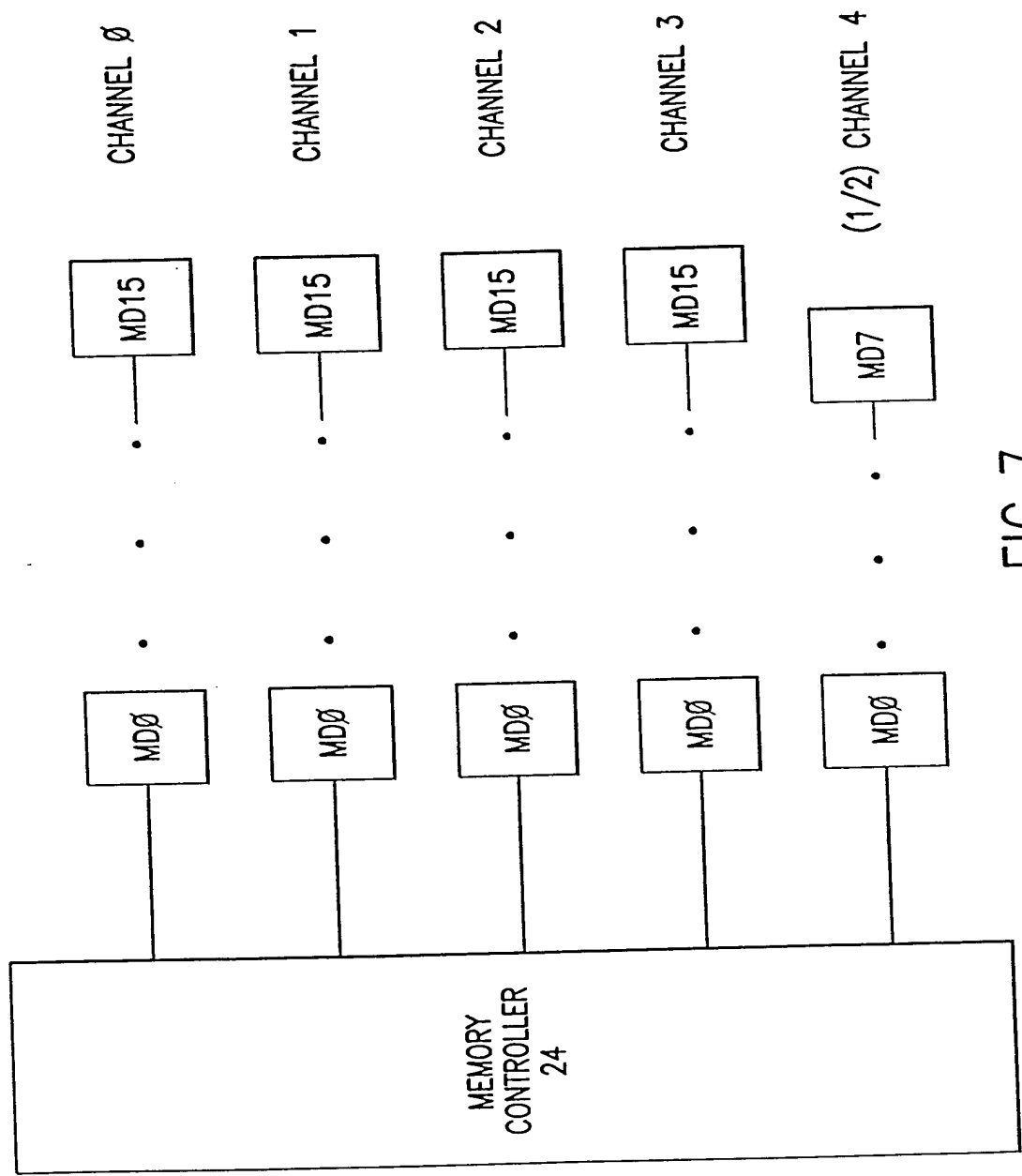


FIG. 7

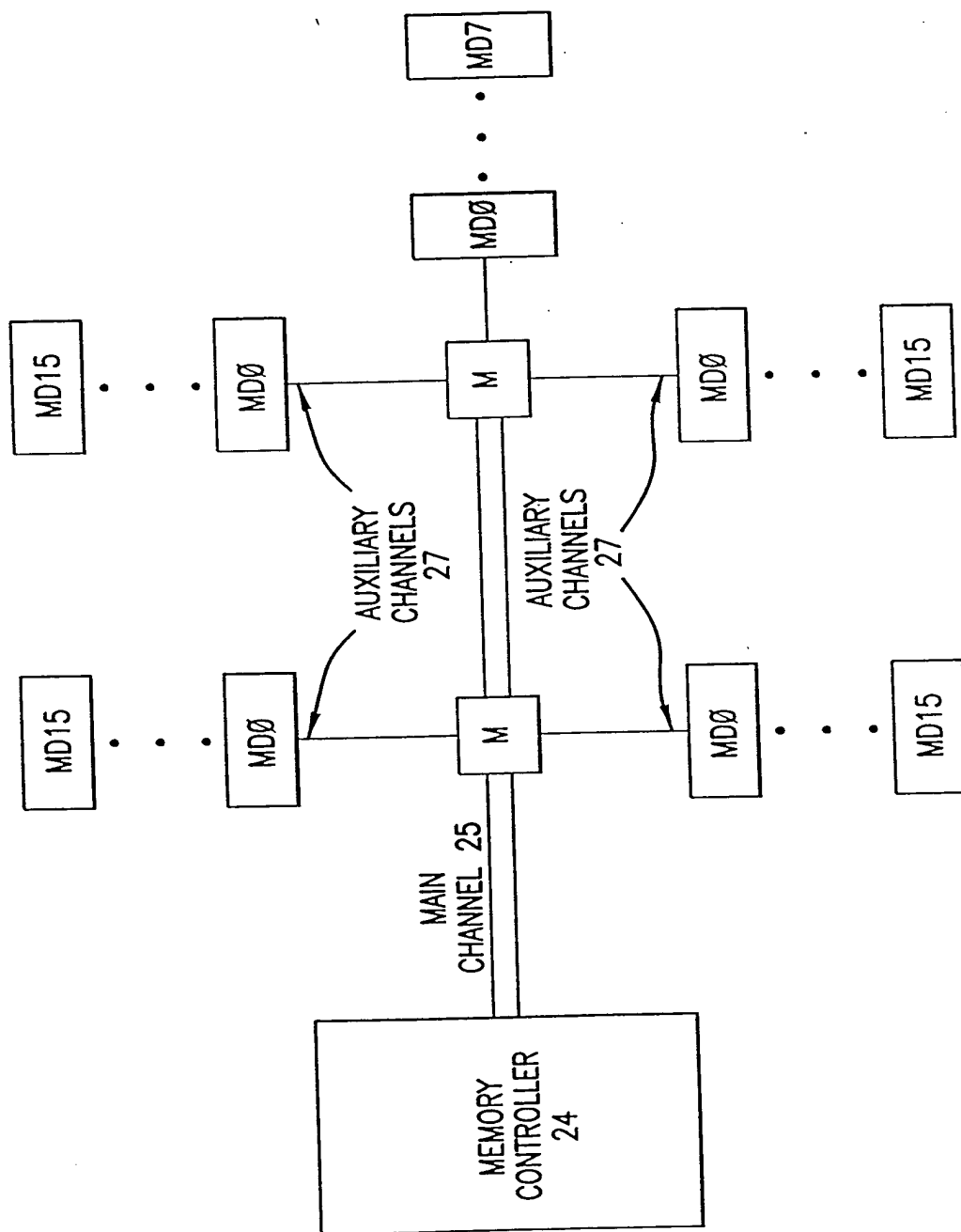


FIG. 8

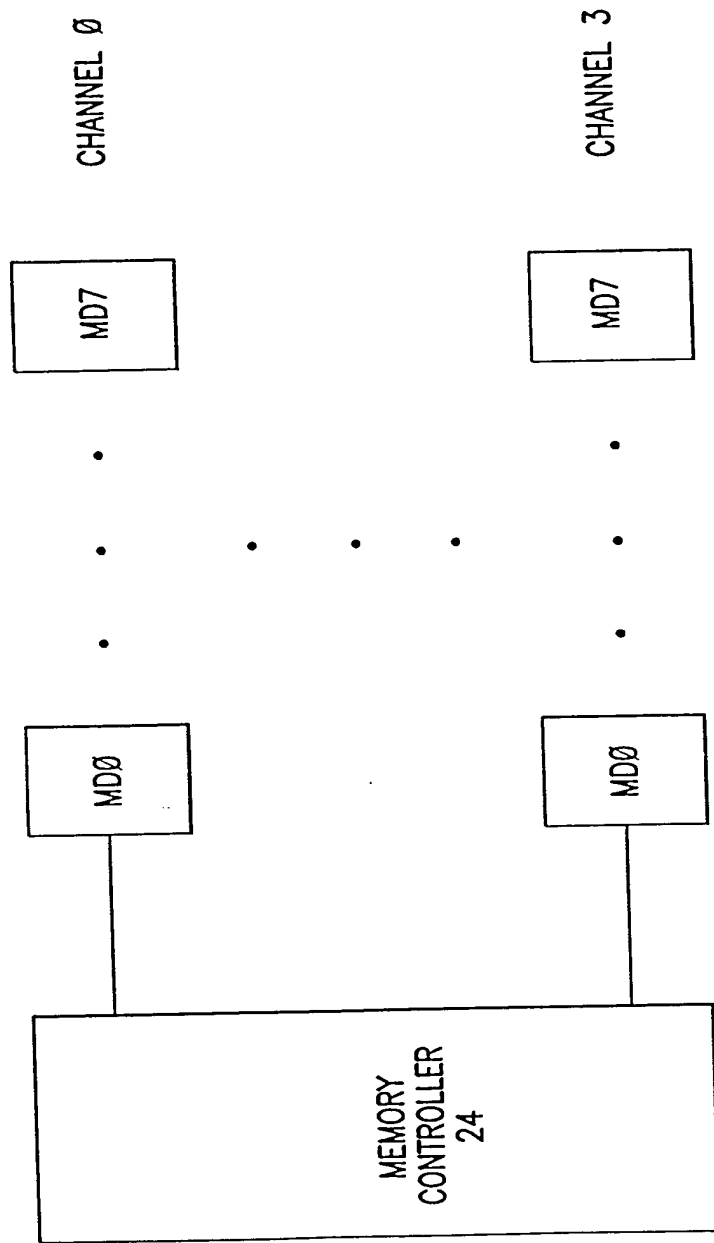


FIG. 9

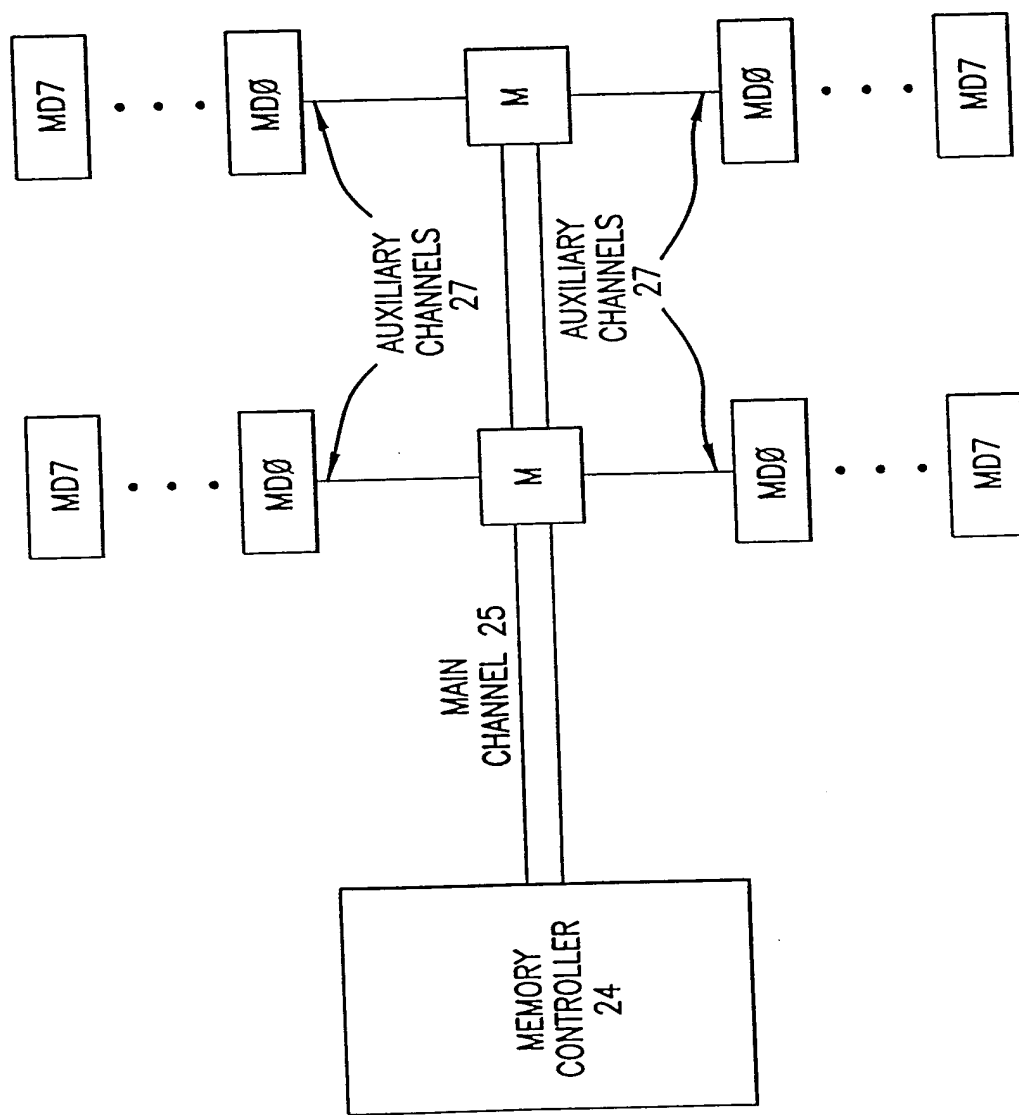


FIG. 10

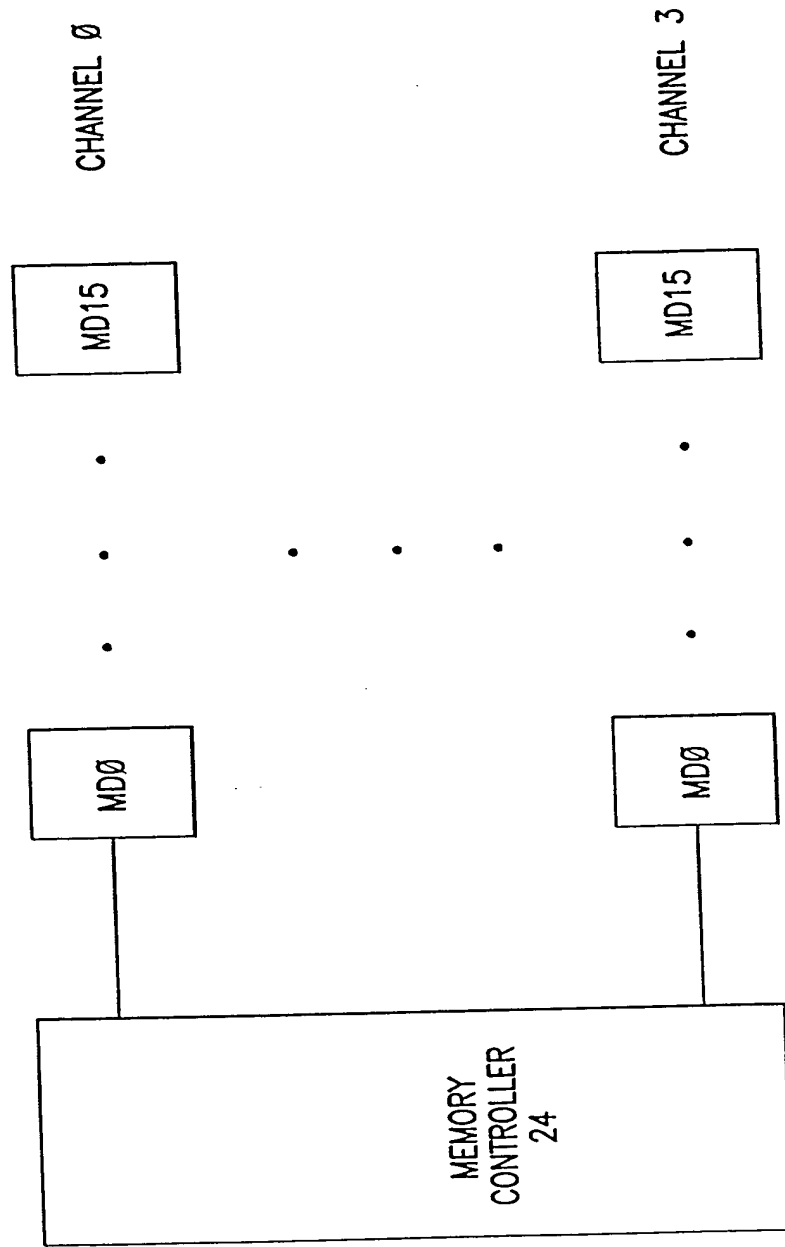


FIG. 11

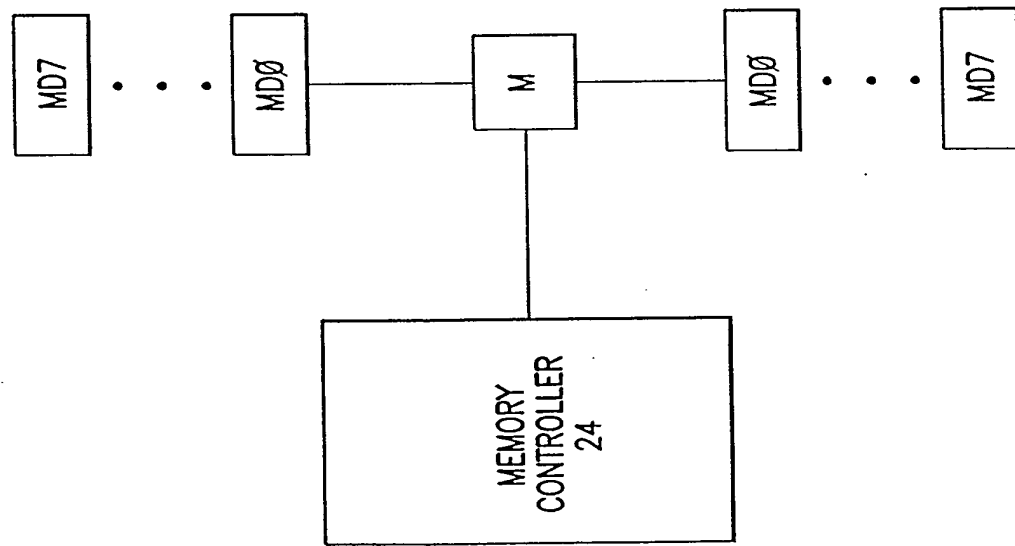


FIG. 12

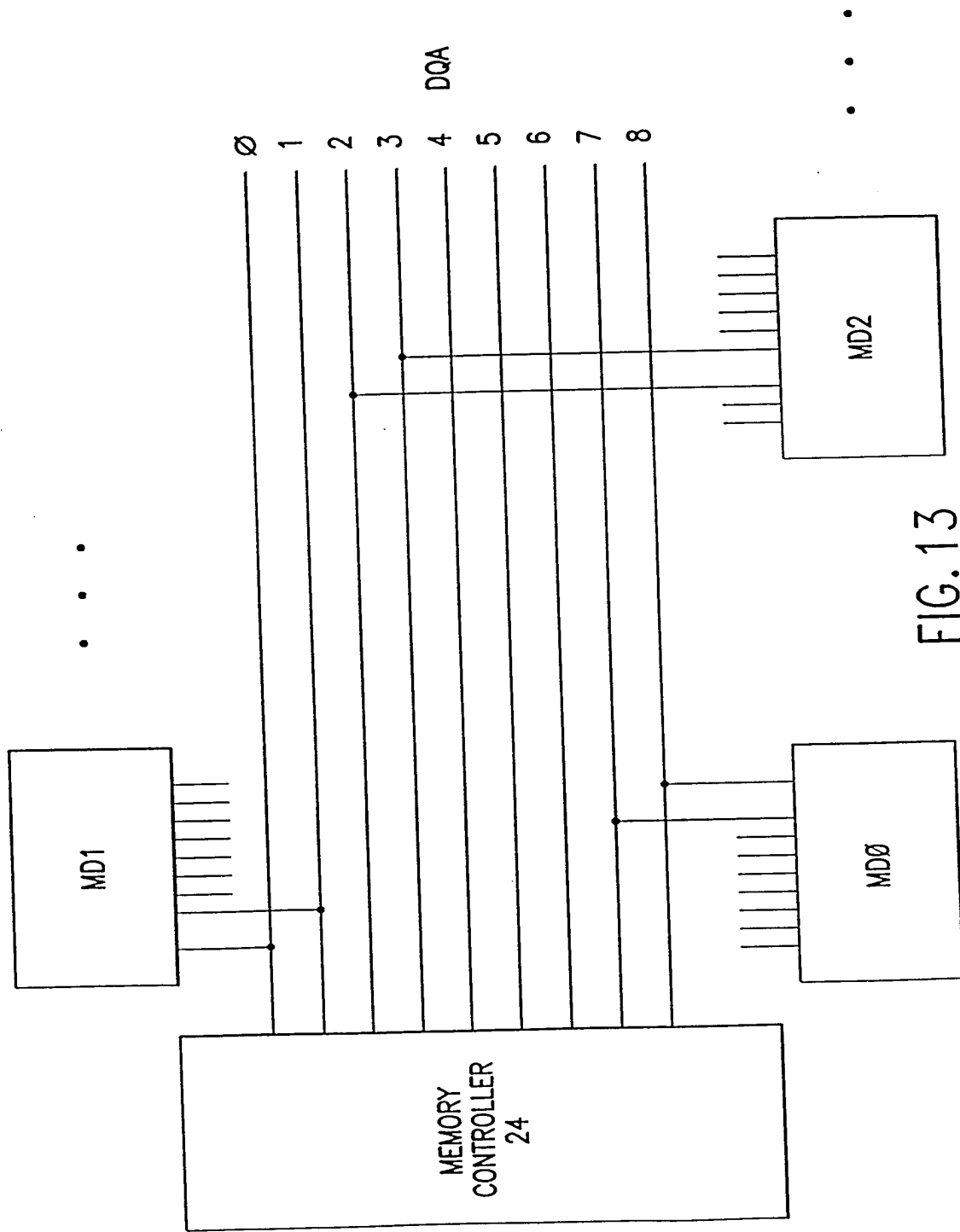


FIG. 13

CYCLE	ROW[2]	ROW[1]	ROW[0]
0	BIT 1 BIT 4	BIT 2 BIT 5	BIT 3
1			
2			
3			

ROW PACKET STRUCTURE

FIG. 14A

CYCLE	COL [4]	COL [3]	COL [2]	COL [1]	COL [0]
0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5
			COPBIT 1	COPBIT 2	
1					
2					
3					

COLUMN PACKET STRUCTURE

FIG. 14B

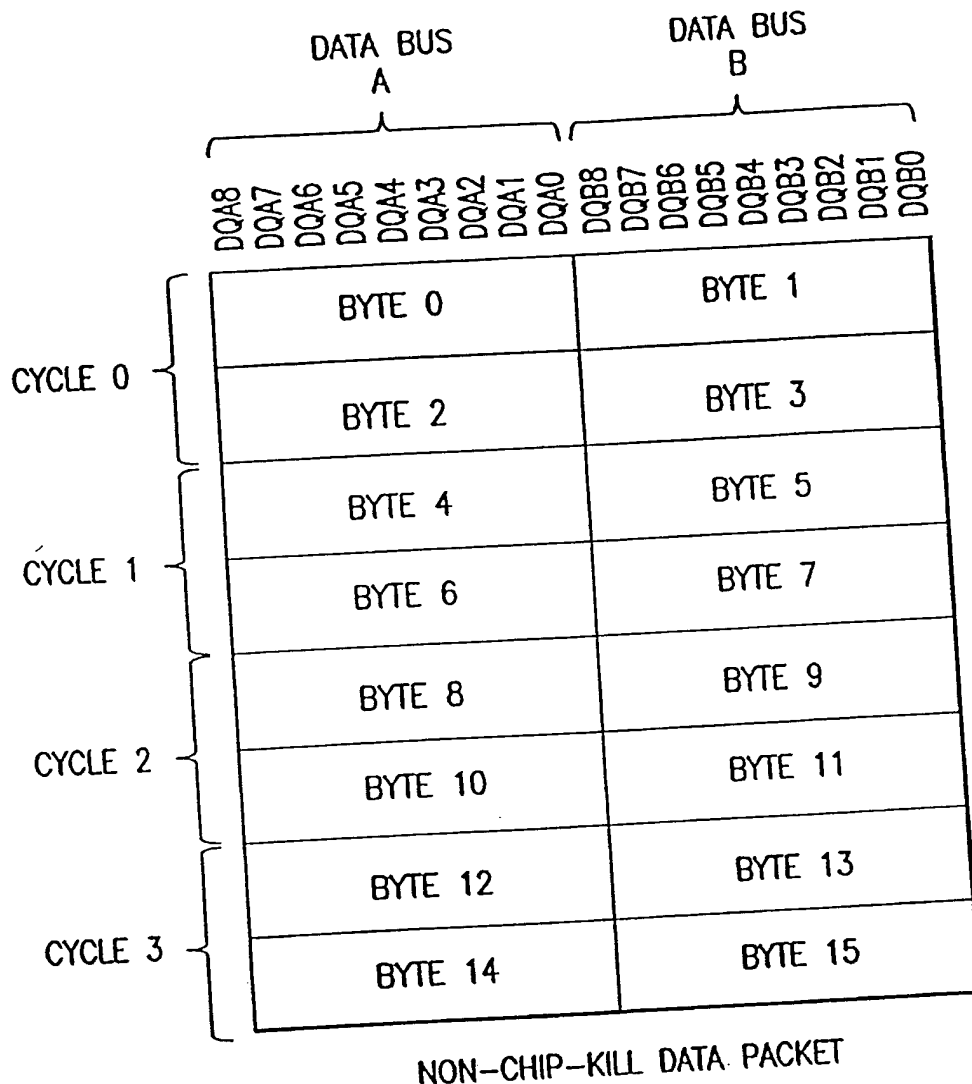
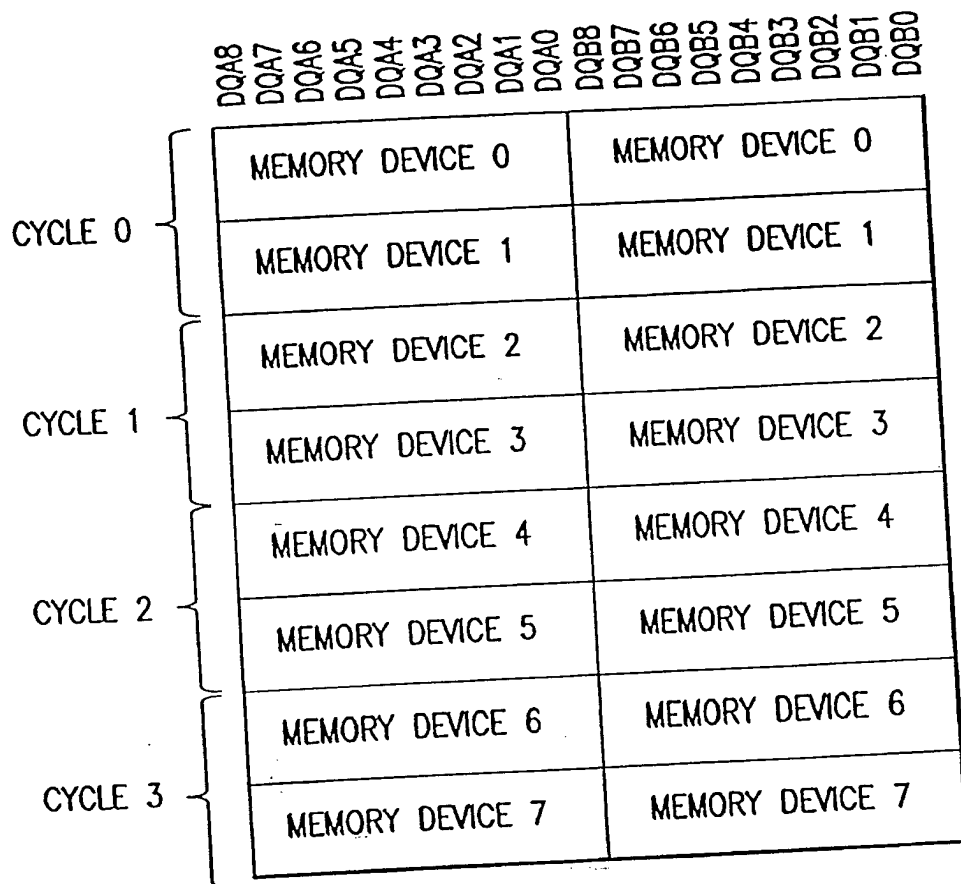


FIG. 15



NON-CHIP-KILL DATA PACKET
CYCLE (TIME) MULTIPLEXING

FIG. 16